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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,164	01/31/2001	Carsten Noeske	Micronas.5873	6108

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,164	NOESKE, CARSTEN	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2005 and 09/19/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 12/13/2005.

2. Claims 1-11 are pending in this application. Claims 1 and 7 are independent claims. This Office Action is made non-final after a RCE filed 12/13/2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4 and 6-10 are rejected under 35 U.S.C. 103(a) as being obvious over Deutsch et al. (U.S. 4,031,377).

Re claim 1, Deutsch et al. disclose in Figure 1 a computing device on a monolithic integrated circuit for multiplying together a digitized multiplier signal value (C or output of 82) and a digitized multiplicand signal value (S or output of 81), computing device comprising: an input interface (81) that receives multiplicand and provides a received multiplicand indicative thereof (80); a first place shifting device (13) that includes a first logical assignment circuit to shift data bits of received multiplicand in response to a first shift command signal (17-21), and provides a first shifted signal indicative thereof (26); a second place shifting device (12) that includes a second logical

assignment circuit to shift data bits of received multiplicand in response to a second shift command signal (16), and provides a second shifted signal indicative thereof (25); means for summing (27) first and second shifted signals (A and B) to provide a summed signal value that is indicative of the product of multiplier and multiplicand (28'); and a control device (14) that receives a signal indicative of multiplier (15), and generates (e.g. col. 2 lines 5-15, col. 2 lines 25-29, and col. 9 lines 3-9), first (16) and second shift command signals (18-21) indicative of multiplier value. Deutsch et al. do not disclose in Figure 1 the first and second means are bi-directionally shifter. However, Deutsch et al. discloses another embodiment the shift circuit would be a bi-directional shifter for either shifting left or right depending on the multiplier factor (e.g. col. 4 lines 5-12). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace the mono-directional shift circuits with the bi-directional shift circuits with functional as cited in Deutsch et al.'s alternative embodiment because it would enable to correctly multiplying with decimal factor (e.g. col. 9 line 60 to col. 10 line 2).

Re claim 2, Deutsch et al. further disclose in Figure 1 a memory device for storing summed signal, and for providing past values of summed signal value (83).

Re claim 3, Deutsch et al. further disclose in Figure 1 means for summing receives and sums a signal value from memory device indicative of a past value of summed signal value with first and second shifted signals to provide summed signal value (83 acts as an accumulator to sum all the terms).

Re claim 4, Deutsch et al. further disclose in Figure 1 first place shifting device (13) comprises a first sign inverter (table III in col. 6) that receives and selectively inverts the sign of received multiplicand (S) to provide a second sign inverted received multiplicand signal that is input to first logical assignment circuit (13) for bit shifting (col. 5 lines 10-15 and table III in col. 6).

Re claim 6, Deutsch et al. further disclose in Figure 1 control unit (14) generates a first sign inversion command signal (17-19) in response to multiplier value, wherein first sign inversion signal is input to first sign inverter to selectively enable the sign inversion (table III in col. 6).

Re claim 7, Deutsch et al. disclose in Figure 1 a monolithic integrated circuit on a monolithic integrated circuit for multiplying together a digitized multiplier signal value and a digitized multiplicand signal value (e.g. abstract wherein multiplier signal value and multiplicand signal value would be 82 and 81 respectively), computing device comprising: an input interface (e.g. 81 and 82) that receives multiplicand and provides a received multiplicand indicative thereof, first means (e.g. 12) for shifting data bits of received multiplicand in response to a first shift command signal, and for providing a first shifted signal indicative thereof; second means (e.g. 13) for shifting data bits of received multiplicand in response to a second shift command signal, and for providing a second shifted signal indicative thereof, means (e.g. 27) for summing first and second shifted signals to provide a summed signal value that is indicative of the product of multiplier and multiplicand (e.g. output of 28 as X = SC); and a control device (e.g. 14) that receives a signal indicative of multiplier that is a binary coded number using canonical

form, and generates, within at least a clock cycle (e.g. col. 2 lines 5-15, col. 2 lines 25-29, and col. 9 lines 3-9), first and second shift command signals (e.g. 16 and 17-21) indicative of multiplier value. Deutsch et al. do not disclose in Figure 1 the first and second means are bi-directionally shifter. However, Deutsch et al. discloses another embodiment the shift circuit would be a bi-directional shifter for either shifting left or right depending on the multiplier factor (e.g. col. 4 lines 5-12). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace the mono-directional shift circuits with the bi-directional shift circuits with functional as cited in Deutsch et al.'s alternative embodiment because it would enable to correctly multiplying with decimal factor (e.g. col. 9 line 60 to col. 10 line 2).

Re claim 8, it is a means claim of claim 2. Thus, claim 8 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 9, it is a means claim of claim 3. Thus, claim 9 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 10, it is a means claim of claim 4. Thus, claim 10 is also rejected under the same rationale in the rejection of rejected claim 4.

5. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being obvious over Deutsch et al. (U.S. 4,031,377), as applied to claim 4 above, in view of Main (U.S. 5,402,369).

Re claim 5, Deutsch et al. do not disclose in Figure 1 a second place shifting device comprises a second sign inverter that receives and inverts the sign of received multiplicand to provide a sign inverted received multiplicand signal that is input to

second logical assignment circuit for bit shifting. However, Main discloses in Figure 1 that the multiplier can be factored as multiple plus or minus terms in col. 5 lines 10-15. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an inverter in the first place shifting device as seen in Main's reference into Deutsch et al.'s reference because it would enable to compute the product faster and more efficient (without the first inverter, the system has to bypass the first place shifting device and subtract in the next clock using the second place shifting device).

Re claim 11, it is a means claim of claim 5. Thus, claim 11 is also rejected under the same rationale in the rejection of rejected claim 5.

Response to Arguments

6. Applicant's arguments filed 12/13/2005 have been fully considered but they are not persuasive.

a. The applicant argues in pages 8-9 for claims 7-10 that it is improper to combine the bi-directional shifter in supposed alternative embodiment with the left shifters to compute the product.

The examiner respectfully believes that it is proper to combine part under alternative embodiment with the reference's invention wherein the bi-directional shifter is placed in cascaded with the left shifters. In another words, it can be generally interpreted the same bi-directional shifter belong to both left shifters which functions as two bi-directional shifter. As clearly disclosed in column 9

line 60 to column 10 line 2, the output of bi-directional shifter 80a is in-placed for the output of 80.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

February 6, 2006

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SUPERVISORY PATENT EXAMINER
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